

U.S. PATENT APPLICATION

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Invention: METHOD OF SEMICONDUCTOR DEVICE FABRICATION

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SPECIFICATION

TITLE OF THE INVENTION
METHOD OF SEMICONDUCTOR DEVICE FABRICATION

BACKGROUND OF THE INVENTION

5 The present invention relates to a method of semiconductor device fabrication using a semiconductor substrate comprising a lattice-strain relaxed silicon germanium layer formed on a silicon substrate or an SOI (silicon-on-insulator) substrate, wherein a lattice strained silicon layer is formed on said silicon germanium
10 layer, or alternatively wherein a lattice strained silicon layer is formed on one or more semiconductor layers formed on said silicon germanium layer.

DESCRIPTION OF THE RELATED ART

15 In the prior art, a semiconductor substrate is known that is fabricated for improving the mobility of carriers (electrons or holes) passing through a channel. That is, a silicon germanium layer 22 having lattice strain is formed into a virtual lattice shape on a silicon substrate 21, while the strain in the silicon germanium layer
20 22 due to lattice constant incommensurate to the silicon substrate 21 is relaxed by introducing misfit dislocations. Then, a silicon layer 24 serving as a cap layer is formed on this strain relaxed silicon germanium layer 22 where the lattice strain is relaxed (Figure 4A). This silicon layer 24 suffers tension from the strain
25 relaxed silicon germanium layer 22 having a larger lattice constant,

and thereby has strain. This causes a change in the band structure, so as to improve the mobility of the carriers.

When a pair of CMOS transistors is fabricated using the semiconductor substrate fabricated as described above, as shown in
5 Figures 4A-4C, 5D, and 5E, the portions for device activity regions in the semiconductor substrate surface are protected with photoresist 26 (Figure 4B), while trenches T2 serving as device isolation grooves are formed by etching in the portions for device isolation regions (Figure 4C). Then, a silicon dioxide film 29
10 serving as an insulation film is embedded in the trenches T2 by TEOS-CVD (tetraethylorthosilicate chemical vapor deposition). After that, the photoresist 26 is removed, and then the silicon dioxide film 29 is flattened by CMP (chemo-mechanical polishing) (Figure 5D).
15 After that, impurities for well formation and for threshold voltage adjustment are introduced into the N-channel MOS transistor region and the P-channel MOS transistor region by ion implantation. Then, similarly to conventional methods of CMOS transistor fabrication, a gate oxide film 30 is formed, and then a
20 polycrystalline silicon film is deposited by CVD. After that, gate electrodes 31 are formed by dry etching (Figure 5E). Then, source-drain regions are formed, so that a pair of CMOS transistors is obtained (see, for example, JP-A 2002-76334).

In this fabrication method, as a result of the etching of the
25 portions for device isolation regions, each trench T2 is formed into a

shape having sharp edge portions E2 in the bottom (Figure 4C).

After that, the silicon dioxide film 29 is embedded in the trench T2

in the state that the edge portions E2 remain sharp. Accordingly,

the silicon dioxide film 29 is formed in a shape corresponding to the

5 trench T2 having sharp edge portions E2 (Figure 5D). Thus, strain

is concentrated on the edge portions E2, so as to induce lattice

defects in the fabrication processes. This causes the problem that

leak current increases between the source region and the well

region not shown so as to affect adversely the electrical

10 characteristics.

In order to avoid this adverse influence, in the formation of

the device isolation regions in the semiconductor substrate, after

the etching of the portions for device isolation regions, thermal

oxidation may be performed on the trench surface so as to round the

15 sharp edge portions in the trench formed by the etching. On the

other hand, in a semiconductor substrate in which a strain relaxed

silicon germanium layer is formed on a silicon substrate and in

which a strained silicon layer is formed on the strain relaxed silicon

germanium layer, the etching of the portions for device isolation

20 regions causes the strain relaxed silicon germanium layer and the

strained silicon layer to be exposed as the side surfaces of the trench.

These strain relaxed silicon germanium layer and strained silicon

layer have different thermal oxidation rates from each other. This

causes non-uniformity in the formed oxide film and hence induces

25 defects, so as to cause the problem of an increase in the leak

current.

SUMMARY OF THE INVENTION

The invention has been devised with considering these
5 situations. An object of the invention is to provide a method of
semiconductor device fabrication in which after the portions for
device isolation regions are etched, a silicon film is deposited on the
substrate, and then the deposited silicon film is oxidized so as to
form a uniform oxide film and round the sharp edge portions of
10 trenches, so that device isolation regions are formed that have high
electrical reliability.

An aspect of the invention is a method of semiconductor
device fabrication using a semiconductor substrate comprising a
lattice-strain relaxed silicon germanium layer and a lattice strained
15 silicon layer formed in this order of mention onto a silicon substrate
or onto a substrate having a silicon layer on the surface thereof,
said method comprising: an etching step of etching the portions for
device isolation regions of said semiconductor substrate so as to
form device isolation grooves; a deposition step of depositing a
20 silicon film on said semiconductor substrate; and an oxidation step
of oxidizing the deposited silicon film.

According to the invention, a semiconductor substrate is
used that comprises a lattice-strain relaxed silicon germanium layer
and a lattice strained silicon layer formed in this order of mention
25 onto a silicon substrate or onto a substrate having a silicon layer on

the surface thereof. Then, the portions for device isolation regions of said semiconductor substrate are etched so as to form device isolation grooves. After that, a silicon film is deposited on said semiconductor substrate. Then, the deposited silicon film is
5 oxidized. By virtue of this method, an oxide film having a uniform thickness is formed on the surfaces of the silicon germanium layer and the silicon layer exposed as the side surfaces of trenches by the etching, while sharp edge portions in the trenches formed by the etching are rounded. As a result, device isolation regions are
10 formed in which the occurrence of leak current is avoided and which have high electrical reliability.

Another aspect of the invention is a method of semiconductor device fabrication using a semiconductor substrate comprising a lattice-strain relaxed silicon germanium layer, one or more
15 semiconductor layers, and a lattice strained silicon layer formed in this order of mention onto a silicon substrate or onto a substrate having a silicon layer on the surface thereof, said method comprising: an etching step of etching the portions for device isolation regions of said semiconductor substrate so as to form
20 device isolation grooves; a deposition step of depositing a silicon film on said semiconductor substrate; and an oxidation step of oxidizing the deposited silicon film.

According to the invention, a semiconductor substrate is used that comprises a lattice-strain relaxed silicon germanium layer,
25 one or more semiconductor layers, and a lattice strained silicon

layer formed in this order of mention onto a silicon substrate or onto a substrate having a silicon layer on the surface thereof. Then, the portions for device isolation regions of said semiconductor substrate are etched so as to form device isolation grooves. After that, a
5 silicon film is deposited on said semiconductor substrate. Then, the deposited silicon film is oxidized. By virtue of this method, an oxide film having a uniform thickness is formed on the surfaces of the silicon germanium layer, the semiconductor layers (on the silicon germanium layer), and the silicon layer exposed by the
10 etching, while sharp edge portions in the trenches formed by the etching are rounded. As a result, device isolation regions are formed in which the occurrence of leak current is avoided and which have high electrical reliability.

Another aspect of the invention is a method of semiconductor
15 device fabrication, wherein in said deposition step, a silicon film of 5 through 10 nm is deposited.

According to the invention, the silicon film deposited on the semiconductor substrate in which device isolation grooves are formed has a thickness of at least 5 nm. This allows the sharp
20 edge portions in the trenches to be rounded at a radius satisfying minimum requirement. Further, the deposited silicon film has a thickness of at most 10 nm. This avoids the formation of an unnecessarily thick oxide film, and hence maintains the detailed structure of the semiconductor device.

25 Another aspect of the invention is a method of semiconductor

device fabrication, wherein in said oxidation step, said deposited silicon film is oxidized completely.

According to the invention, the silicon film deposited on the semiconductor substrate in which device isolation grooves are
5 formed is oxidized completely. By virtue of this, a uniform oxide film is formed on the surfaces of the silicon germanium layer and the silicon layer (or on the surfaces of the silicon germanium layer, the semiconductor layers (on the silicon germanium layer), and the silicon layer) exposed as the side surfaces of trenches. This avoids
10 possible defects that could occur owing to the remained interface between an unoxidized silicon film and the side surface of the trench in case that the surface of the deposited silicon film were oxidized partly.

Another aspect of the invention is a method of semiconductor
15 device fabrication, further comprising the step of depositing a protective film for protecting portions for device activity regions onto the surface of said semiconductor substrate before said etching step.

According to the invention, before said etching step, a
20 protective film composed of silicon nitride or the like is deposited on the surface of the semiconductor substrate, so as to protect, from the etching, the portions for device activity regions of the semiconductor substrate covered by the protective film. Further, the protective film serves as a stopper in the step of polishing the
25 device isolation film embedded in the etched device isolation grooves

in a subsequent step, so as to protect the portions for device activity regions of the semiconductor substrate covered by the protective film.

The above and further objects and features of the invention
5 will more fully be apparent from the following detailed description with accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1D and 2E-2G are schematic diagrams
10 illustrating a method of semiconductor device fabrication according to the invention.

Figure 3 is an enlarged view of the vicinity of a trench.

Figures 4A-4C and 5D-5E are schematic diagrams
illustrating a prior art method of semiconductor device fabrication.
15

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is described below with reference to the drawings illustrating the embodiments. An example of
20 embodiment of fabricating a pair of CMOS transistors by the following processes is described below with reference to the schematic diagrams of Figures 1A-2G.

As a preprocess, a p-type (100) silicon substrate 1 is treated by high-temperature sulfuric acid cleaning and RCA cleaning.
25 Then, the natural oxide film on the silicon substrate 1 is removed

with 5% diluted hydrofluoric acid. Then, a silicon germanium layer 2 having a germanium concentration of 30% and a thickness of 150 nm is formed on the silicon substrate 1 by epitaxial growth at 500°C using germanium hydride (GeH.sub.4) and silicon hydride (SiH.sub.4) in a low-pressure chemical vapor deposition (LP-CVD) system. After that, hydrogen ions are implanted into the semiconductor substrate composed of the silicon substrate 1 and the silicon germanium layer 2 under the conditions of implantation energy of 18 keV, dose of 3×10^{16} H⁺/cm², and implantation angle of 7°. Then, the semiconductor substrate is treated by high-temperature sulfuric acid cleaning and RCA cleaning. After the cleaning, the semiconductor substrate is annealed in nitrogen atmosphere at 800°C for 10 min in an electric anneal furnace.

As a result, small cavities called micro cavities having a size of 10 nm or the like are formed in the vicinity of the peak of the distribution of the implanted hydrogen ions which is located at 20-50 nm in the direction from the interface between the silicon germanium layer 2 and the silicon substrate 1 to the silicon substrate 1. Stacking faults caused by the formation of the micro cavities slide so as to generate misfit dislocations in the interface between the silicon germanium layer 2 and the silicon substrate 1. This relaxes the strain in the crystal lattice of the silicon germanium layer 2.

A silicon germanium layer 3 serving as a semiconductor layer having a germanium concentration of 30% and a thickness of

300 nm is formed by epitaxial growth on the surface of the above-mentioned strain relaxed silicon germanium layer 2 where the strain has been relaxed. Then, a silicon layer 4 serving as a channel, through which carriers pass, having a thickness of 20 nm is formed on the silicon germanium layer 3 by epitaxial growth. At that time, the silicon germanium layer 3 has a larger lattice constant than the silicon layer 4. Accordingly, the silicon layer 4 suffers tension from the silicon germanium layer 3, so that strain appears in the silicon layer 4.

10 A protective film 5 having a thickness of 500-1500 nm for protecting portions for device activity regions in a subsequent process is deposited by CVD on the surface of the semiconductor substrate S formed as described above (Figure 1A). The protective film 5 is composed of silicon nitride(Si.sub.3N.sub.4).

15 After that, photoresist 6 is spin-coated into a thickness of 500-1500 nm on the protective film 5. Then, the photoresist 6 is processed by optical exposure in an i-line stepper provided with a photomask for device isolation region (such as STI and LOCOS) formation used in ordinary LSI fabrication. The photoresist 6 is
20 then developed with an alkaline developer. As a result, a photoresist pattern is formed by the photoresist 6 remaining on the protective film 5 surface in the portions for device activity regions (Figure 1B).

 After that, the protective film 5 in the portions for device
25 isolation regions is removed by reactive ion etching using the

photoresist 6 remaining on the protective film 5 surface as a photomask. Then, trenches T are formed in the device isolation regions of the semiconductor substrate S by reactive ion etching using the remaining protective film 5 and photoresist 6 as a photomask (Figure 1C). The formed trenches T have sharp edge portions E in the bottom (shown in the left-hand side part of Figure 3).

After that, the photoresist 6 remaining on the protective film 5 surface is removed. Then, a polycrystalline silicon film 7 having a thickness of 5-10 nm is deposited by CVD onto the entirety of the exposed surfaces, that is, the surface (top surface) and the exposed surfaces (side surfaces) of the protective film 5 as well as the side surfaces and the bottom surfaces of the trenches T (Figure 1D).

After that, the deposited polycrystalline silicon film 7 is dry-oxidized so as to form a silicon dioxide film 8 (Figure 2E). For example, when the deposited polycrystalline silicon film 7 has a thickness of 5 nm, the polycrystalline silicon film is oxidized completely by dry oxidation at 950-1050°C for 10-30 min.

As a result, the sharp edge portions E in the trenches T which are shown in an enlarged view in the left-hand side part of Figure 3 are rounded when the polycrystalline silicon film deposited on the side surfaces and the bottom surfaces of the trenches T is oxidized into silicon dioxide completely as shown in an enlarged view in the right-hand side part of the figure.

Then, a silicon dioxide film 9 serving as an insulation film is

embedded in the trenches T by TEOS-CVD. After that, the silicon dioxide film 9 is polished and flattened by CMP using the protective film 5 as a stopper. After the flattening, the protective film 5 is removed (Figure 2F).

5 After that, impurities for well formation and for threshold voltage adjustment are introduced into the N-channel MOS transistor region and the P-channel MOS transistor region by ion implantation (not shown). Then, similarly to conventional methods of CMOS transistor fabrication, a gate oxide film 10 is formed, and
10 then a polycrystalline silicon film is deposited by CVD. After that, gate electrodes 11 are formed by the dry etching of the deposited polycrystalline silicon film (Figure 2G). Then, source-drain regions are formed. As a result, a pair of CMOS transistors is obtained according to the method of semiconductor device fabrication of the
15 invention.

 In the present embodiment, a semiconductor substrate S has been used that comprises a strain relaxed silicon germanium layer 2 in which the strain is relaxed and which is formed on a silicon substrate 1, wherein another silicon germanium layer 3 serving as a
20 semiconductor layer is formed on the strain relaxed silicon germanium layer 2, and wherein a strained silicon layer 4 having strain is formed on the silicon germanium layer 3. However, the invention is not restricted to this and may be as follows. That is, the semiconductor substrate may be such that a strained silicon
25 layer 4 is formed on the strain relaxed silicon germanium layer 2.

Further, the semiconductor substrate may be such that another semiconductor layer is formed between the strain relaxed silicon germanium layer 2 and the silicon germanium layer 3 or alternatively between the silicon germanium layer 3 and the strained silicon layer 4. Furthermore, the silicon film deposited after the formation of the trenches T is not restricted to a polycrystalline silicon film, and may be another type of film composed solely of silicon, such as an amorphous silicon film and a single crystal silicon film.

10 In the present embodiment, a semiconductor substrate S has been used that is composed of a silicon substrate 1 on which a strain relaxed silicon germanium layer 2, a strained silicon layer 4, and the like are formed. However, the silicon substrate 1 may be replaced by a SOI substrate having a silicon layer on the surface thereof. Even in this case, CMOS transistors are fabricated that are similar to those obtained by using the silicon substrate 1.

 According to the invention, a semiconductor substrate is used that comprises a lattice-strain relaxed silicon germanium layer formed on a silicon substrate or on a substrate having a silicon layer on the surface thereof, wherein a lattice strained silicon layer is formed said silicon germanium layer. Then, the portions for device isolation regions of said semiconductor substrate are etched so as to form device isolation grooves. After that, a silicon film is deposited on said semiconductor substrate. Then, the deposited silicon film is oxidized. By virtue of this method, an oxide film having a

uniform thickness is formed on the surfaces of the silicon germanium layer and the silicon layer exposed as the side surfaces of trenches by the etching, while sharp edge portions in the trenches formed by the etching are rounded. As a result, device isolation regions are formed in which the occurrence of leak current is avoided and which have high electrical reliability.

According to the invention, a semiconductor substrate is used that comprises a lattice-strain relaxed silicon germanium layer formed on a silicon substrate or on a substrate having a silicon layer on the surface thereof, wherein a lattice strained silicon layer is formed on one or more semiconductor layers formed on said silicon germanium layer. Then, the portions for device isolation regions of said semiconductor substrate are etched so as to form device isolation grooves. After that, a silicon film is deposited on said semiconductor substrate. Then, the deposited silicon film is oxidized. By virtue of this method, an oxide film having a uniform thickness is formed on the surfaces of the silicon germanium layer, the semiconductor layers (on the silicon germanium layer), and the silicon layer exposed by the etching, while sharp edge portions in the trenches formed by the etching are rounded. As a result, device isolation regions are formed in which the occurrence of leak current is avoided and which have high electrical reliability.

According to the invention, the silicon film deposited on the semiconductor substrate in which device isolation grooves are formed has a thickness of at least 5 nm. This allows the sharp

edge portions in the trenches to be rounded at a radius satisfying minimum requirement. Further, the deposited silicon film has a thickness of at most 10 nm. This avoids the formation of an unnecessarily thick oxide film, and hence maintains the detailed
5 structure of the semiconductor device.

According to the invention, the silicon film deposited on the semiconductor substrate in which device isolation grooves are formed is oxidized completely. By virtue of this, a uniform oxide film is formed on the surfaces of the silicon germanium layer and
10 the silicon layer (or on the surfaces of the silicon germanium layer, the semiconductor layers (on the silicon germanium layer), and the silicon layer) exposed as the side surfaces of trenches. This avoids possible defects that could occur owing to the remained interface between an unoxidized silicon film and the side surface of the
15 trench in case that the surface of the deposited silicon film were oxidized partly.

According to the invention, before said etching step, a protective film composed of silicon nitride or the like is deposited on the surface of the semiconductor substrate, so as to protect, from
20 the etching, the portions for device activity regions of the semiconductor substrate covered by the protective film. Further, the protective film serves as a stopper in the step of polishing the device isolation film embedded in the etched device isolation grooves in a subsequent step, so as to protect the portions for device activity
25 regions of the semiconductor substrate covered by the protective

film.

As this invention may be embodied in several forms without departing from the spirit of essential characteristics thereof, the present embodiment is therefore illustrative and not restrictive,
5 since the scope of the invention is defined by the appended claims rather than by the description preceding them, and all changes that fall within metes and bounds of the claims, or equivalence of such metes and bounds thereof are therefore intended to be embraced by the claims.